Plasma-induced defect-site generation in si substrate and its impact on performance degradation in scaled MOSFETs

AUTHOR(S):

Eriguchi, Koji; Nakakubo, Yoshinori; Matsuda, Asahiko; Takao, Yoshinori; Ono, Kouichi

CITATION:

Eriguchi, Koji ...[et al]. Plasma-induced defect-site generation in si substrate and its impact on performance degradation in scaled MOSFETs. IEEE Electron Device Letters 2009, 30(12): 1275-1277: 5313889.

ISSUE DATE:

2009-12

URL:

http://hdl.handle.net/2433/89515

Plasma-Induced Defect-Site Generation in Si Substrate and Its Impact on Performance Degradation in Scaled MOSFETs

Koji Eriguchi, Yoshinori Nakakubo, Asahiko Matsuda, Yoshinori Takao, and Kouichi Ono

***Abstract*—Plasma-induced ion-bombardment damage was studied in terms of defect sites created underneath the exposed Si surface. From the shift of capacitance–voltage (C–V) curves, the defect sites were found to capture carriers (being negatively charged in the case of an Ar plasma exposure). This results in a change of the effective impurity-doping density and the profile. We also report that the defect density depends on the energy of ions from plasma. A simplified and quantitative model is proposed for the drain–current degradation induced by the series-resistance increase by the damage. The relationship derived between the defect density and the drain–current degradation is verified by device simulations. The proposed model is useful to predict the device performance change from plasma process parameters.**

***Index Terms*—Capacitance, defect site, device simulation, drain current, plasma-induced damage (PID).**

I. Introduction

With regard to the present-day process technology, plasma processing is widely used for fabricating finer patterns with anisotropic features in advanced MOSFETs. In general, plasma-induced damage (PID) is classified based on the mechanism into charging damage, physical damage, and radiation damage [1]. Physical damage is commonly associated with the damage induced by high-energy ion bombardment on material surfaces. Damage to the Si surface occurs during gate-, offset-, and sidewall-spacer etch processes, resulting in Si recess in the source/drain (S/D) extension region [2], [3] and the creation of underlying defect site [4]. Recently, the relationship between the recess depth (d_R) and threshold-voltage shift was modeled and confirmed by device simulations, where the defect site was neglected [3]. However, the defect sites created (Si vacancy, displaced Si, interstitial, dangling bond, etc. [5]) are believed to be electrically active and possible sources of device degradation. In some cases, the volume density was estimated to be on the order of 10^{19} cm^{-3} [4]. Moreover, these sites are difficult to remove by wet-etch and annealing processes [4], [6]. Kokura *et al.* [6] reported that the defects generated by CF_4 plasma exposures changed the impurity-doping profile, leading to an increase in sheet resistance. Although the plasma-induced defects in Si substrate have been analyzed by many researchers [6]–[10], there have been few reports on the effects on device performance. Therefore, it is extremely important to understand the correlation between defect density and device parameters. In this letter, we focus on the electrical feature and density of defect site created by an Ar plasma. A relationship between the density and the drain–current degradation is clarified by considering a plasma-induced resistance increase. The model is verified by device simulations.

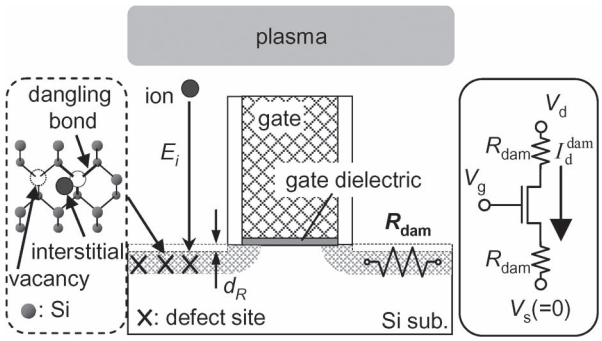

Fig. 1. Schematic illustration of damaged layer formation by plasma exposure, leading to Si recess and defect-site creation. An offset-spacer etch process is assumed in this figure. The damaged region (with defect sites) increases the series resistance in the source/drain extension (SDE) region.

II. Impacts of Plasma-Induced Physical Damage

A. Defect-Site Generation During Plasma Processing

Fig. 1 shows mechanisms of plasma-induced physical damage. This figure shows an offset-spacer etch process. As shown, the damaged layer with defect sites is formed by an impact of energetic ions accelerated in the plasma sheath. As analyzed by ellipsometry and molecular dynamic simulations [3], [11], the damaged layer consists of two regions, i.e., the surface and interfacial layers (in this letter, we will abbreviate them to SL and IL, respectively). The SL is composed of SiO_2, due to oxidation of heavily damaged region, and the IL, partially oxidized or disordered Si, which is identified by spectroscopic ellipsometry (SE) as a mixed layer consisting of crystalline Si and SiO_2 phases [3], [11]. As expected, during the subsequent wet-etch step, the SL and a portion of the IL are stripped off. However, as deduced from the results by Kokura *et al.* [6], some defects are still present and expected to induce the variation

Manuscript received July 14, 2009; revised September 15, 2009. First published November 6, 2009; current version published November 20, 2009. This work was supported in part by the Semiconductor Technology Academic Research Center and in part by the Japan Society for the Promotion of Science under a Grant-in-Aid for Scientific Research (B) 20360329. The review of this letter was arranged by Editor K. De Meyer.

The authors are with Kyoto University, Kyoto 606-8501, Japan (e-mail: eriguchi@kuaero.kyoto-u.ac.jp; y.nakakubo@ks7.ecs.kyoto-u.ac.jp; asahiko@phys.mbox.media.kyoto-u.ac.jp; takao@kuaero.kyoto-u.ac.jp; ono@kuaero.kyoto-u.ac.jp).

Digital Object Identifier 10.1109/LED.2009.2033726

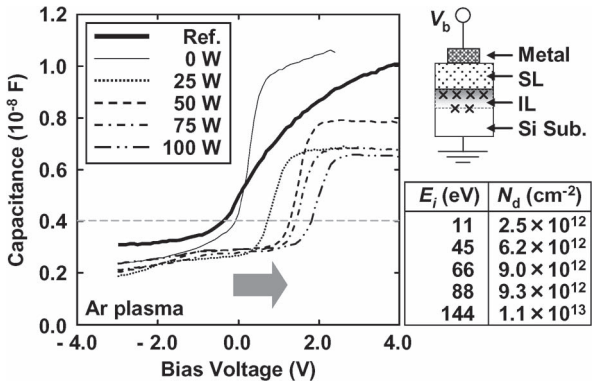

Fig. 2. Capacitance–voltage curves of metal/SL/IL/Si structure obtained by a mercury probe for various bias powers $P_{\rm RF}$. The table lists the average ion energy $E_i(= q(V_p - V_{\rm dc}))$ and the calculated areal density of defect site (N_d).

of impurity-doping profile as a carrier trapping site, because they are not fully recovered by the subsequent annealing. Thus, this mechanism is believed to exacerbate the variation of device performance.

B. Analysis of Defect-Site Density

In this section, we experimentally clarify the electrical characteristics and density range of defect sites created by the plasma. N-type (100) Si ($\sim$0.02 $\Omega\cdot$cm) was exposed to an inductively coupled plasma (ICP) with Ar gas mixture for 30 s. A sample without the exposure served as a reference. The source ICP power was 300 W, and the pressure was 2.0×10^{-2} torr. RF bias at 13.56 MHz $(P_{\rm RF})$ was applied with various powers ranging from 0 to 100 W. Plasma diagnostics determined the plasma potential $(V_p \sim 11.0$ V) and the average self dc bias $(V_{\rm dc} < 0)$. The present plasma configuration results in a constant ion flux (Γ_i) to Si substrate [12] for all conditions $(\Gamma_i \sim 5.0\times10^{16}$ cm$^{-2}\cdot$s$^{-1})$. Since the bias frequency is high enough, the ion energy distribution function has a narrow energy spectrum [13]. Thus, we define the average impacting ion energy E_i as $q(V_p - V_{\rm dc})$, where q is electronic charge. Therefore, the incident ion energy was varied throughout the experiments with Γ_i being constant.

We conducted capacitance–voltage $(C$–$V)$ measurement to clarify the electrical feature of defects by using a mercury probe without inducing any additional damage by forming an electrode. As shown in Fig. 2, we evaluated the bias-voltage shift (ΔV_b) in C–V curves at 0.4×10^{-8} F for various plasma-exposed samples. As shown, ΔV_b increases with an increase in $P_{\rm RF}$. In addition, in the present case, V_b shifts toward the positive direction. This implies that the defects are able to capture negative charges (electrons). Thus, the defects are considered to trap or detrap electrons in accordance with applied biases, i.e., in this case, electron trapping sites [4], [13]. Further study is required to ascertain the energy level of these defects in detail. By assuming that the defect sites are located within the IL, one can estimate an areal defect density N_d from the thickness of SL and IL [14]. The results are listed in the table shown in Fig. 2. As shown, the estimated N_d increases with an increase in E_i. From the IL thickness obtained by SE ($\sim$2 nm) [3], the estimated areal density range of N_d corresponds to an average volume density on the order of $\sim10^{19}$ cm^{-3}, which is consistent with the results by other methods [4]. Thus, we focus on the peak volume density of defect which ranges from 0 to 10^{19} cm^{-3}.

C. Model for Drain–Current Degradation By Defect Site

In order to clarify the plasma-induced device performance degradation, we consider the case shown in Fig. 1 without the recess $(d_R = 0)$. As discussed earlier, the defects are carrier trapping sites, thus change the doping density and its profile in the S/D extension (SDE) regions, resulting in increase in the series resistance $(R_{\rm dam})$, as shown in Fig. 1. By taking into account the voltage drop by the series resistance [15], one can write the drain current for damaged devices with $R_{\rm dam}$ as

$$I_d^{\rm dam} = \frac{\mu C_{\rm ox} W}{L_{\rm eff}} \frac{(V_g - V_{\rm th} - V_d/2)\left(V_d - 2I_d^{\rm dam}R_{\rm dam}\right)}{1 + \theta\cdot\left(V_g - V_{\rm th} - I_d^{\rm dam}R_{\rm dam}\right)} \tag{1}$$

where $L_{\rm eff}$ is the effective channel length, μ is the effective surface mobility, $C_{\rm ox}$ is the dielectric capacitance, W is the channel width, θ is a mobility-degradation coefficient, V_g is the gate voltage, and $V_{\rm th}$ is the threshold voltage. Since the PID under consideration does not affect the mobility in channel region, one can let $\theta = 0$. In the case of a low-drain bias case $(V_d \ll (V_g - V_{\rm th}))$, the drain current is described as

$$I_d^{\rm dam} = \frac{\beta' V_d}{1 + 2\beta' R_{\rm dam}} \tag{2}$$

where $\beta' = \mu C_{\rm ox} W/L_{\rm eff}\cdot(V_g - V_{\rm th} - V_d/2)$. For simplicity, in (2), we define $R_{\rm dam} = A\times(n_0 - n_{\rm dam})^{-1}$ [14], where n_0 and $n_{\rm dam}$ are the effective dopant density in the SDE without PID and the effective defect-site density, respectively. Note that n_0 depends on the peak concentration and the junction depth (X_j), and $n_{\rm dam}$ on the peak defect-site density (or N_d) and the distribution depth $(X_{\rm dam})$. A is the SDE structure-dependent constant. From the experimental result [3], as aforementioned, $X_{\rm dam}$ is a few nanometers; thus, $X_j \gg X_{\rm dam}$. This means that $n_0 \gg n_{\rm dam}$, i.e., $(2A\beta' + n_0) \gg n_{\rm dam}$. Therefore, one can make an approximation for the drain–current degradation in (2) as

$$I_d^{\rm dam} \approx \frac{\beta' V_d}{2A\beta' + n_0}\left(n_0 - \frac{2A\beta'}{2A\beta' + n_0} n_{\rm dam}\right). \tag{3}$$

This equation indicates that $I_d^{\rm dam}$ depends linearly on $n_{\rm dam}$.

D. Device Simulations

In order to investigate the device performance degradation and to verify the relationship in (3), we performed 2-D technology computer-aided design (TCAD) simulations for n-channel MOSFETs. Gate dielectric thickness was 2 nm. The substrate doping was 5×10^{17} cm^{-3}. The peak concentration of SD region was 1×10^{20} cm^{-3}. The junction depth of SD was 120 nm. The peak concentration of SDE region $(n_{0\,\max})$ was

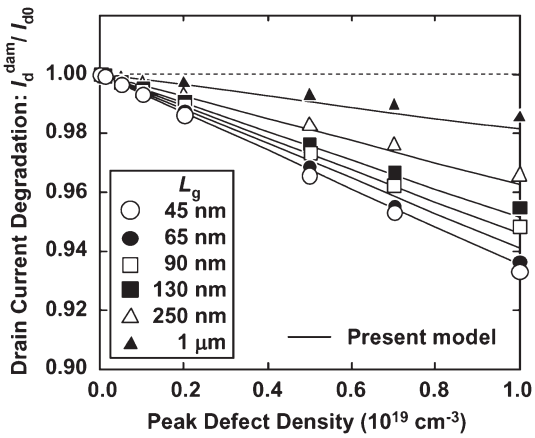

Fig. 3. Normalized drain–current degradation as a function of defect-site density for devices with various gate lengths. I_{d0} is the drain current of device without PID. ($V_g = 1.2$ V, $V_d = 0.05$ V, $X_{\rm dam} = 2.0$ nm).

1×10^{19} cm^{-3} at the Si surface. X_j was 26 nm. At X_j, the density was 1×10^{18} cm^{-3}, and a Gaussian profile was employed. The defect site by PID was introduced as the counter doping [6] with its peak value $(n_{d\,\max})$ at the Si surface. $X_{\rm dam}$ was 2.0 nm. At $X_{\rm dam}$, the density is $0.1 \times n_{d\,\max}$. We adopted a Gaussian profile for the distribution tail. This assumption is based on the impinging ion profile obtained by an etching profile simulation [1], [4], [16]. This is also consistent with the damage distribution model by ion implantation [5], [17]. Based on a Gaussian profile, n_0 and $n_{\rm dam}$ are in proportion to $n_{0\,\max}$ and $n_{d\,\max}$, respectively. Details of other parameters used in this letter are described elsewhere [3]. Fig. 3 shows the simulated results. As shown, the drain current decreases with the increase in $n_{d\,\max}$, and the slope becomes steeper as the gate length (L_g) becomes shorter. Fig. 3 also shows the results estimated by (3). In this calculation, $L_{\rm eff} = L_g - \Delta L (= 5$ nm) and $\mu = 210$ cm$^2 \cdot$ V$^{-1} \cdot$ s^{-1} were used. The n_0 and $n_{\rm dam}$ in (3) are derived from $n_{0\,\max}$, $n_{d\,\max}$, and the profiles (X_j and $X_{\rm dam}$). Other parameters were determined from TCAD data for the references with various L_g. The good agreement between TCAD data and (3) is shown. Since the defect-site density can be determined from the PID analyses as performed in this letter, one can predict the drain–current degradation from the PID data by using (3).

III. Conclusion

A linear relationship between defect-site density and drain current has been proposed. The model was verified by the device simulations. The proposed quantitative model is useful to estimate the device performance degradation from plasma parameters (Γ_i and E_i) via N_d and IL thickness. Moreover, one can quantify the damage by the device parameter change.

Acknowledgment

The authors would like to thank Dr. H. Ohta of the University of California, Santa Barbara, for his helpful discussion.

References

[1] K. Eriguchi and K. Ono, "Quantitative and comparative characterizations of plasma process-induced damage in advanced metal–oxide–semiconductor devices," *J. Phys. D, Appl. Phys.*, vol. 41, no. 2, p. 024 002, Jan. 2008.

[2] T. Ohchi, S. Kobayashi, M. Fukasawa, K. Kugimiya, T. Kinoshita, T. Takizawa, S. Hamaguchi, Y. Kamide, and T. Tatsumi, "Reducing damage to Si substrates during gate etching processes," *Jpn. J. Appl. Phys.*, vol. 47, no. 7, pp. 5324–5326, Jul. 2008.

[3] K. Eriguchi, A. Matsuda, Y. Nakakubo, M. Kamei, H. Ohta, and K. Ono, "Effects of plasma-induced Si recess structure on n-MOSFET performance degradation," *IEEE Electron Device Lett.*, vol. 30, no. 7, pp. 712–714, Jul. 2009.

[4] K. Eriguchi, Y. Nakakubo, A. Matsuda, M. Kamei, H. Ohta, H. Nakagawa, S. Hayashi, S. Noda, K. Ishikawa, M. Yoshimaru, and K. Ono, "A new framework for performance prediction of advanced MOSFETs with plasma-induced recess structure and latent defect site," in *IEDM Tech. Dig.*, 2008, pp. 443–446.

[5] J. D. Plummer, M. Deal, and P. B. Griffin, *Silicon VLSI Technology, Fundamentals, Practice and Modeling*. Englewood Cliffs, NJ: Prentice-Hall, 2000.

[6] H. Kokura, K. Okabe, M. Nakaishi, and M. Miyajima, "Plasma induced damage on ultra shallow junction in spacer etching," in *Proc. Symp. Dry Process*, 2005, pp. 27–28.

[7] I. W. Wu, R. A. Street, and J. J. C. Mikkelsen, "Damage to shallow n^+/p and p^+/n junctions by $CHF_3 + CO_2$ reactive ion etching," *J. Appl. Phys.*, vol. 63, no. 5, pp. 1628–1635, Mar. 1988.

[8] X. C. Mu, S. J. Fonash, A. Rohatgi, and J. Rieger, "Comparison of the damage and contamination produced by CF_4 and CF_4/H_2 reactive ion etching: The role of hydrogen," *Appl. Phys. Lett.*, vol. 48, no. 17, pp. 1147–1149, Apr. 1986.

[9] A. Henry, O. O. Awadelkarim, J. L. Lindstrom, and G. S. Oehrlein, "Electrical studies on plasma and reactive-ion-etched silicon," *J. Appl. Phys.*, vol. 66, no. 11, pp. 5388–5393, Dec. 1989.

[10] S. A. Vitale and B. A. Smith, "Reduction of silicon recess caused by plasma oxidation during high-density plasma polysilicon gate etching," *J. Vac. Sci. Technol. B, Microelectron. Process. Phenom.*, vol. 21, no. 5, pp. 2205–2211, Sep. 2003.

[11] A. Matsuda, Y. Nakakubo, Y. Ueda, H. Ohta, K. Eriguchi, and K. Ono, "Significance of interface layer between surface layer and Si substrate in plasma-exposed structures and its impacts on plasma-induced damage analysis," in *Proc. Ext. Abstr. Solid State Devices Mater.*, 2008, pp. 358–359.

[12] M. A. Lieberman and A. J. Lichtenberg, *Principles of Plasma Discharges and Materials Processing*, 2nd ed. New York: Wiley-Interscience, 2005.

[13] A. M. Goodman, "Metal–Semiconductor barrier height measurement by the differential capacitance method—One carrier system," *J. Appl. Phys.*, vol. 34, no. 2, pp. 329–338, Feb. 1963.

[14] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. New York: Wiley-Interscience, 1981.

[15] C. C. McAndrew and P. A. Layman, "MOSFET effective channel length, threshold voltage, and series resistance determination by robust optimization," *IEEE Trans. Electron Devices*, vol. 39, no. 10, pp. 2298–2311, Oct. 1992.

[16] Y. Osano, M. Mori, N. Itabashi, K. Takahashi, K. Eriguchi, and K. Ono, "A model analysis of feature profile evolution and microscopic uniformity during polysilicon gate etching in Cl_2/O_2 plasmas," *Jpn. J. Appl. Phys.*, vol. 45, no. 10B, pp. 8157–8162, 2006.

[17] G. Hobler and S. Selberherr, "Two-dimensional modeling of ion implantation induced point defects," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 7, no. 2, pp. 174–180, Feb. 1988.